10400 Eaton Place
Suite 312
FAIRFAX, VA
Phone: (703) 385-5200
Fax: (703) 385-5080

KEATING & BENNETT LLP

Fax

RECEIVED
CENTRAL FAX CENTER
MAY 17 2005

To:	Examiner Brock	**From:**	Peter Medley
Fax:	703-872-9306	**Date:**	May 17, 2005
Phone:	571-272-1722	**Pages:**	16
Re:	09/658,732 36856.919	**CC:**	

•Comments:

Examiner Brock,

Please find attached hereto the following documents for the above-identified application:

1) Reply Brief;

2) Request for Oral Hearing; and

3) Credit Card Form PTO-2038.

Respectfully submitted,

Peter Medley
for
Keating & Bennett, LLP
(Registration Number 56,125)

PATENT
36856.919

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Makoto INAI et al. Serial No.: 09/658,732 Filed: September 11, 2000 Title: FIELD-EFFECT SEMICONDUCTOR DEVICE	Art Unit: 2815 Examiner: P. Brock II

REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants are filing this Reply Brief in response to the Examiner's Answer, dated March 17, 2005, in connection with the above identified application.

ARGUMENTS:

In the Examiner's Answer of March 17, 2005, the Examiner maintained the rejection of claims 1-10 and 12-15 under 35 U.S.C. §103(a) as being unpatentable over Sawada et al. ("A Super Low-Noise AlGaAs/InGaAs/GaAs DC-HFET with 0.15 μm Gate-Length") in view of Enoki et al. ("Delay Time Analysis for 0.4- to 5- μm -Gate InAlAs-InGaAs HEMT's").

The Examiner has improperly indicated certain issues as admitted

In the second full paragraph on page 9 of the Examiner's Answer, the Examiner alleged, "Because these issues are not disputed, they are treated as admitted by Applicant." Applicants respectfully submit that just because Applicants have not addressed certain issues, those issues should not be treated as admitted.

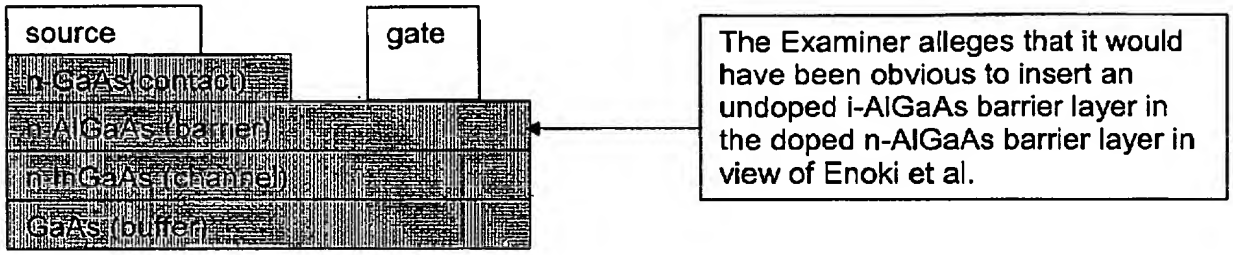
The Examiner's proposed modification of Sawada et al. will increase the resistance of the modified semiconductor device

The Examiner has taken two positions on whether or not his proposed modification to the device in **Fig. 1** of Sawada et al. will increase the resistance. The Examiner has alleged that the series resistance of the modified Sawada et al./Enoki et al. semiconductor device is not "unduly" or "unsatisfactorily" increased in the paragraph on page 11 of the Examiner's Answer, and has alleged that the series resistance of the modified Sawada et al./Enoki et al. semiconductor device is reduced in the paragraph bridging pages 19 and 20 and in the last full sentence on page 21 of the Examiner's Answer.

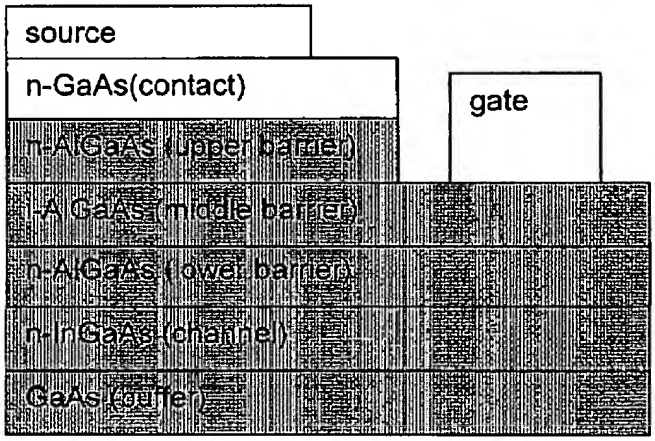
In paragraph c. on page 6 of the Examiner's Answer, the Examiner stated, "It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the Sawada [et al.] n-AlGaAs barrier layer by providing an additional undoped layer between the top and bottom portions (or restated, by temporarily stopping and restarting the n-type impurity dopant supply during the growth of the barrier layer) ... ." Applicants have provided the following two schematic drawings to

clearly illustrate the Examiner's proposed modification of the semiconductor device illustrated in Fig. 1 of Sawada et al.:

Fig. 1 of Sawada et al.



Modified Fig. 1 of Sawada et al.



As clearly seen from the above two drawings, the Examiner's proposed modification includes inserting a non-doped i-AlGaAs barrier layer into the n-doped n-AlGaAs barrier layer.

The Examiner has also characterized the modification as replacing the entire barrier layer of the device in **Fig. 1** of Sawada et al. with the entire n-i-n homojunction barrier. See, *e.g.*, the first paragraph on page 12 of the Examiner's Answer, "Sawada [et al.]'s figure 6 reinforces the combination in that it further proves that the highly doped barrier layers of Enoki [et al.] must be employed in Sawada [et al.], figure 1, when using the undoped barrier layer of Enoki [et al.] in the combination ... ." This alternative characterization results in the exact same structure as the above modified **Fig. 1**

Sawada et al. Further, all of Applicants' arguments presented in this Appeal Brief apply equally well to both of the Examiner's characterizations of the modifications.

An n-type dopant is considered to be an electron donor because it increases the number of free electrons, or electrons that contribute to the conductance of the semiconductor device. That is, by inserting an undoped i-AlGaAs (or by temporarily stopping and restarting the n-type impurity dopant supply during the growth of the barrier layer) into the n-doped n-AlGaAs barrier layer of the semiconductor device of **Fig. 1** of Sawada et al., the number of free electrons is reduced in the barrier layer. Thus, the Examiner's proposed modification to the semiconductor device of Sawada et al. will increase the resistance of the modified Sawada et al./Enoki et al. semiconductor device compared to the unmodified semiconductor device of Sawada et al. because the number of free electrons in the barrier layer has been reduced.

The Examiner has failed to provide any evidence that the resistance of the modified device is not "unsatisfactorily high" or "unduly increased"

In the last paragraph on page 7 of the Office Action dated May 18, 2004, the Examiner alleged:

> As such, the further inclusion of an undoped layer composed of the same material as the rest of Sawada [et al.]'s barrier layer would not cause the barrier to possess unsatisfactorily high resistance because the additional presence of the upper, highly n-doped region of the AlGaAs barrier layer that forms a junction with the GaAs [source/drain] contact layers in Sawada [et al.] would sufficiently reduce the [source/drain] series resistance to allow the Sawada [et al.] HFET to operate as intended, as taught by Enoki [et al].

In the paragraph on page 11 in the section labeled "First:" of the Examiner's Answer, the Examiner alleged, "By including in Sawada [et al.] all three of the barrier layers of Enoki's n-i-n homojunction barrier layer scheme the series resistance is not unduly increased, as would be the case if the combination only included the undoped barrier layer of Enoki [et al.] in Sawada [et al]."

While the Examiner has admitted in these portions that the addition of the undoped i-AlGaAs layer increases the series resistance, the Examiner has failed to

provide any objective evidence to support the allegation that this increase is offset to the extent that either the series resistance is not "unsatisfactorily high" or that the series resistance would not be "unduly increased."

Because the Examiner has failed to provide any objective evidence to support either of these allegations, Applicants respectfully submit that it is improper for the Examiner to rely upon these allegations to establish a *prima facie* case of obviousness. Further, Applicants respectfully submit that the Examiner has failed to prove that one of ordinary skill in the art would have considered the proposed modification of the device of **Fig. 1** of Sawada et al. in view of the teachings of Enoki et al. to have a reasonable expectation of success in view of the increased series resistance of the modified device.

The Examiner has failed to establish a prima facie case of obviousness

As explained in MPEP § 2142, "[t]he legal concept of *prima facie* obviousness is a procedural tool of examination which applies broadly to all arts. It allocates who has the burden of going forward with production of evidence in each step of the examination process. ... The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

In order to establish a *prima facie* case of obviousness, the Examiner must show that:

1) there is some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
2) there is a reasonable expectation of success; and
3) the prior art reference (or references when combined) must teach or suggest all the claim limitations.

MPEP § 2143. Further, the Federal Circuit has held, "[The factual inquiry whether to combine references] must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Lee, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002). That is, the Examiner

must provide objective evidence in order to establish each of the three requirements explained above.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness because he has failed to provide objective evidence, as further discussed below, to support (1) the alleged motivation to combine Sawada et al. and Enoki et al. and (2) the reasonable expectation of success of combining Sawada et al. and Enoki et al. Further, because the Examiner has failed to establish a *prima facie* case of obviousness, it is improper for the Examiner to place the burden upon Applicants to produce evidence that proves that the Examiner's unsupported allegations are incorrect.

In the paragraph bridging pages 17 and 18, the Examiner stated:

> Appellant only argues that the examiner has failed to provide any evidence to support this allegation. The problem with Appellant's argument is threefold. First, Appellant had never requested that such evidence be provided during prosecution. Because it was first raised on appeal, Appellant's request for further evidence is untimely. Second, various references of record (e.g., Sawada [et al.] USPAT 5,404,032) do substantiate this allegation. Third, Appellant is not arguing that the Examiner failed to provide a basis for the reasonable expectation of success. Rather, Appellant implicitly acknowledges that the Examiner provided a basis for the reasonable expectation of success, and thereby did what was legally required to establish a prima facie case of obviousness.

With respect to the Examiner's first point, there is absolutely no support for the Examiner's position in the laws, rules, or holdings in the case law. MPEP § 2144.03, Section C., which is directed to taking Official Notice, states, "If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate. If the traverse was inadequate, the examiner should include an explanation as to why it was inadequate." Because the Examiner has failed to take Official Notice of the disputed allegations, the Examiner's position, that

Applicants' request that the Examiner fully satisfy his obligation to establish a *prima facie* case of obviousness is untimely, is unreasonable because it is not supported by any law, rule, or holding in the case law. Further, the Examiner is clearly admitting on the record that he has failed to provide objective evidence to establish a *prima facie* case of obviousness and is clearly indicating a refusal to satisfy the requirements of establishing a *prima facie* case of obviousness.

With respect to the Examiner's second point, as further discussed below, Applicants respectfully submit that U.S. Patent No. 5,404,032 fails to provide the support required to establish a *prima facie* case of obviousness.

With respect to the Examiner's third point, Applicants do argue that the Examiner has failed provide objective evidence that establishes a reasonable chance of success.

Also in the paragraph bridging pages 17 and 18 of the Examiner's Answer, the Examiner stated, "Rather, Appellant implicitly acknowledges that the Examiner provided a basis for the reasonable expectation of success, and thereby did what was legally required to establish a prima facie case of obviousness." Applicants cannot disagree more with this statement. At absolutely no place in the prosecution history of the present application have the Applicants even hinted that they thought or acknowledged that the Examiner had established a *prima facie* case of obviousness.

The Examiner has failed to establish that increasing the Schottky barrier is proper motivation for combining Sawada et al. and Enoki et al.

In paragraph c. on page 6 of the Examiner's Answer, the Examiner repeated the allegation that it would have been obvious to combine Sawada et al. and Enoki et al. "for the purpose of enhancing[, or increasing,] the Schottky barrier of the gate."

The Examiner has failed to provide any objective evidence that the inclusion of an undoped i-AlGaAs layer in the barrier layer of Sawada et al. will increase the Schottky barrier

First, in the paragraph bridging pages 13 and 14, the Examiner has made a series of allegations that are not supported by any objective evidence. Thus, Applicants

respectfully submit that none of these allegations should be considered in determining obviousness.

Second, the Examiner has alleged in the first full paragraph on page 14 of the Examiner's Answer that the Examiner does not need to provide any evidence that the inclusion of an undoped i-AlGaAs layer in the barrier layer of Sawada et al. will increase the Schottky barrier because claim 1 does not recite "any specific III-V material." The Examiner has misunderstood Applicants' argument. Applicants are arguing that the Examiner has improperly combined Sawada et al. and Enoki et al. and are not arguing the combination of Sawada et al. and Enoki et al. lacks some specific feature recited in claim 1.

Third, in the paragraph bridging pages 16 and 17 of the Examiner's Answer, the Examiner alleged:

> An example that one of ordinary skill in the art would impress the teaching of Enoki [et al.] on a broader concept of III-V semiconductor devices can be found in figures 2 and 13, with the supporting text thereof, of United States Patent number 5,404,032 (made of record in the PTO-892 filed December 5,2001, see appendix A attached hereto). These figures clearly show HEMT[, or High Electron Mobility Transistor, which is a type of HFET] structures based on both AlGaAs-GaAs (figure 2, with a AlGaAs barrier layer) and InP (figure 13, with a InAlAs barrier layer) systems. It is noted that Enoki [et al.] teaches an In-P based HEMT (see the introduction, section I of Enoki [et al.], page 502) and that Sawada [et al.] teaches an AlGaAs-GaAs based HEMT (see the first line of the abstract of Sawada [et al.]). Thus, one of ordinary skill in the art, when considering such known art as the '032 reference, would recognize that Enoki [et al.]'s teachings-of a three-layer, n-i-n homojunction barrier structure scheme and it's benefits over a single n-layer barrier structure scheme-have general applicability to HFET barriers composed of various conventional Group III-V material systems, even though Enoki [et al.] provides an example of only one particular III-V material system.

However, no portion, including those portions relied upon by the Examiner, of U.S. Patent No. 5,404,032 teaches or suggest that the inclusion of an undoped i-AlGaAs between two doped layers of n-AlGaAs and in contact with a AuGe/Ni/Au metal would increase the Schottky barrier. The portion of U.S. Patent No. 5,404,032 relied upon by the Examiner only teaches that structures based on both AlGaAs-GaAs and InP

systems can be used to manufacture a device with two modes of electron transport. As with Enoki et al., the Examiner alleges that U.S. Patent No. 5,404,032 provides a very broad teaching (that AlGaAs-GaAs and InP systems are equivalent in every way) based upon very specific teachings in U.S. Patent No. 5,404,032.

Thus, Applicants respectfully submit that the Examiner has failed to provide any objective evidence that the inclusion of an undoped i-AlGaAs layer in the barrier layer of Sawada et al. would increase the Schottky barrier.

In the paragraph bridging pages 16 and 17 of the Examiner's Answer, the Examiner stated, "Appellant has not provided any proof that this broader concept is not true," and in the paragraph bridging pages 17 and 18 of the Examiner's Answer, the Examiner stated, "... it should be noted that the burden has shifted to the appellant to prove that this is not well known and a physical property of III-V semiconductor materials. ... As an aside, it is noteworthy that Appellant has not provided any evidence refuting this allegation. In fact, Appellant has not even alleged that this allegation is in any way inaccurate."

As explained above, it is the Examiner who must provide objective evidence that his proposed motivation is proper. Because the Examiner has failed to establish a *prima facie* case of obviousness, it is improper for the Examiner to place the burden of production of evidence on Applicants.

The Examiner has failed to provide any objective evidence that one of ordinary skill in the art would have desired to increase the Schottky barrier of the device of **Fig. 1** of Sawada et al.

In the last full paragraph on page 15 of the Examiner's Answer, the Examiner has alleged, "One of ordinary skill would recognize that enhancing the Schottky gate while simultaneously decreasing series resistance in the source [and] drain regions is desirable in the device of Sawada [et al.] based on the teachings of Enoki [et al]."

First, in the first full paragraph on page 6 of the Office Action dated May 18, 2004, the Examiner corrected Applicants' inadvertent statement that "enhanced the Schottky barrier" meant to decrease the Schottky barrier.

Second, in the last paragraph on page 7 of the Office Action dated May 18, 2004, the Examiner stated, "Enoki [et al.] teaches that the inclusion of an undoped layer in the middle of the barrier—to which the gate is in direct, Schottky contact—enhances (or increases) the Schottky barrier."

That is, the Examiner has clearly admitted that the Enoki et al. uses the term "enhance" to mean make higher and not to mean make better. Thus, when Enoki et al. states, "The undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal," Enoki et al. is only making a conclusion concerning the Schottky barrier (that it is increased) and is not suggesting that increasing the Schottky barrier is desirable. Further, assuming *arguendo* that Enoki et al. teaches that increasing the Schottky barrier is desirable in the device shown in **Fig. 1** of Enoki et al., the Examiner has failed to provide any evidence that one of ordinary skill in the art would have considered it desirable to increase the Schottky barrier in the device shown in **Fig. 1** of Sawada et al.

In the last paragraph on page 15 of the Examiner's Answer, the Examiner stated, "The burden is on the appellant to prove that the motivation fails. The appellant has not provided any evidence that the barrier layer of Enoki [et al.] would not benefit the device of Sawada [et al]."

As explained above, it is the Examiner who must provide objective evidence that his proposed motivation is proper. Because the Examiner has failed to establish a *prima facie* case of obviousness, it is improper for the Examiner to place the burden of production of evidence on Applicants.

Thus, Applicants respectfully submit that the motivation "of enhancing[, or increasing,] the Schottky barrier of the gate" is improper.

The Examiner has failed to establish that the reduction of the series resistance is proper motivation for combining Sawada et al. and Enoki et al.

In paragraph c. on page 6 of the Examiner's Answer, the Examiner repeated the allegation that it would have been obvious to combine Sawada et al. and Enoki et al.

"for the purpose of ... providing a source/drain series resistance that is reduced relative to if the upper portion of the barrier was undoped, as taught by Enoki ... ."

As can be clearly seen from examining the first schematic drawing above and **Fig. 1** of Sawada et al., the upper portion of the unmodified device of **Fig. 1** of Sawada et al. is an n-doped n-AlGaAs layer, not an undoped layer. That is, the Examiner is suggesting a modification of **Fig. 1** of Sawada et al. to achieve a benefit (reduced resistance) that the device of **Fig. 1** of Sawada et al. already has because the upper portion of the barrier layer of the unmodified device is already n-doped.

Thus, Applicants respectfully submit that the motivation of "providing a source/drain series resistance that is reduced relative to if the upper portion of the barrier was undoped" is improper.

The Examiner has failed to establish that obviating additional masking steps is proper motivation for combining Sawada et al. and Enoki et al.

In paragraph c. on page 6 of the Examiner's Answer, the Examiner repeated the allegation that it would have been obvious to combine Sawada et al. and Enoki et al. "for the purpose of providing both of these advantages [, of increased Schottky barrier and reduced resistance relative to if the upper portion of the barrier was undoped,] while simultaneously obviating the need for the additional masking steps that would be required to achieve the structure of Sawada [et al.]'s **Fig. 6** embodiment wherein the dopant implant is provided for only the [source/drain] regions." Further, in the first paragraph on page 12 of the Examiner's Answer, the Examiner alleged, "Sawada [et al.]'s figure 6 reinforces the combination in that it further proves that the highly doped barrier layers of Enoki [et al.] must be employed in Sawada [et al.], figure 1, when using the undoped barrier layer of Enoki [et al.] in the combination, so that the resistance is reduced in the source drain regions."

First, as explained by the Examiner in the paragraph bridging pages 14 and 15 of the Examiner's Answer, the height of the Schottky barrier is determined by the doping concentration of the semiconductor layer that the gate is in direct contact with. That is,

the height of the Schottky barrier does not depend upon the method by which the semiconductor device is manufactured.

Second, as discussed in the paragraph bridging pages 10 and 11 of the Appeal Brief, the device of **Fig. 6** of Sawada et al. fails to teach or suggest a contact layer. Thus, the device of **Fig. 6** of Sawada et al. necessarily fails to teach or suggest the advantage of reduced source/drain series resistance of an n-doped upper portion of the barrier layer that is in direct contact with the contact layer relative to if the upper portion of the barrier layer was undoped. See the paragraph on page 11 of the Examiner's Answer ("[The barrier would not possess unsatisfactorily high resistance] because the additional presence of the upper, highly n-doped region of the AlGaAs barrier layer that forms a junction with the GaAs source-drain (S/D) contact layers in Sawada [et al.] would sufficiently reduce the S/D series resistance ...").

Third, the Examiner has failed to address the fact that, while the implantation technique used to manufacture the device of **Fig. 6** of Sawada et al. might include an additional masking step, the step of forming a contact layer is omitted in the manufacture of the device of **Fig. 6** of Sawada et al.

Fourth, Applicants respectfully submit that it appears that the reduced resistance referred to with respect to the device of **Fig. 6** of Sawada et al. is because of the lack of a contact layer and not because the upper portion of the barrier layer that is in direct contact with a contact layer is doped.

Thus, Applicants respectfully submit that the motivation of "providing both of these advantages while simultaneously obviating the need for the additional masking steps that would be required to achieve the structure of Sawada [et al.]'s **Fig. 6**" is improper.

The Examiner has failed to establish proper motivation for combining Sawada et al. and Enoki et al.

Applicants respectfully submit that each part of the Examiner's proposed motivation to combine Sawada et al. and Enoki et al. is improper, as discussed above. Thus, Applicants respectfully submit that the Examiner has failed to provide proper

motivation for modifying the device of **Fig. 1** of Sawada et al. in view of the teachings of Enoki et al.

Claims 1-18 are Allowable over the Prior Art

Accordingly, Applicants respectfully submit the rejection of claims 1-10 and 12-15 under 35 U.S.C. §103(a) as being unpatentable over Sawada et al. in view of Enoki et al. should be reversed and that claims 1-18 are clearly patentable over Sawada et al. in view of Enoki et al.

Respectfully submitted,

Date: May 17, 2005

/Peter Medley 56,125/
Attorney for Applicants
Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

Peter Medley
Registration No. 56,125

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080